ARGUMENTS/REMARKS

Applicants would like to thank the examiner for the careful consideration given the present application. The application has been carefully reviewed in light of the Office action, and amended as necessary to more clearly and particularly describe and claim the subject matter which applicants regard as the invention.

The examiner objects to the drawings for having non-English alphabet and for improper line, letter, or number thicknesses. Formal drawings having English letters have been submitted with this response as an attachment.

In the specification, the examiner generally objected to the specification. The Examiner says that the specification is not "clear, concise and exact" as required by 35 U.S.C. §112, first paragraph. The statute actually states that the specification should be written in "such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same". Applicant maintains that the specification is sufficiently "clear, concise and exact" that one skilled in the art would be able to make and use the same, and thus the specification meets the statutory requirement. However, applicant has amended those sections specifically objected to by the Examiner.

Claims 1-28 remain in this application. Claims 29-30 have been added.

The examiner objected to claims 3, 8 & 15 for various informalities. These claims have been amended, making the objections moot.

Claims 1 & 28 were rejected under 35 U.S.C. §112, second paragraph. Specifically, claims 1 & 28 were rejected for indefiniteness due to improper antecedent basis. Amendments to claims 1 and 28 make the rejections moot.

Further, claim 1 was also rejected by the examiner under the same statute for being incomplete. Applicant does not understand the Examiner's rejection. It appears that the Examiner wants applicant to add an additional step to the claim, to wit an "electromagnetic interference analyzing step...." Applicant notes that all of the steps of the claim are part of a method for "analyzing the amount of electromagnetic interference arising in an LSI by means of performing a logic simulation" as stated in the preamble, and thus no such step as

recommended is necessary for completeness. Thus, the Examiner should withdraw this rejection. Applicant requests that the Examiner clarify this rejection with specificity if it is not withdrawn.

Claims 1 & 28 were rejected under 35 U.S.C. §102(a) as being anticipated by Hayashi *et al.* ("EMI Noise Analysis Under ASIC Design Environment"). For the following reasons, the rejection is respectfully traversed.

Hayashi teaches only a simplification model for an electric source mesh (see page 18, col. 2, para. 4 to page 19, col. 1, para. 2). In contrast, the language of claims 1 and 28 recited calculating the amount of instantaneous current using a gate-level current analysis method, and modeling a current waveform corresponding to the amount of instantaneous electric current.

Hayashi presupposes a realization at the transistor level. The reference merely states the *potential* of a gate-level realization, but does not teach any. The reference teaches only an EMS noise analysis system carried out at the *transistor* level, and does not teach operability at the gate level. Thus, Hayashi does not enable a gate-level analysis method.

Furthermore, Hayashi teaches that a transistor level simulation is necessary for a voltage/current calculation using its source mesh. In contrast, the invention is capable of very fast analysis.

In the invention, in order to calculate a current noise of an entire chip, a *gate level* calculation method is utilized, making it possible to analyze the circuit *before* the layout is generated. Hayashi requires that the layout *already* be generated, because it teaches a *transistor* level analysis. Thus, the invention provides an evaluation of EMI noise caused by LSI currents at an earlier stage of design than is possible with the Hayashi method. Further, the invention makes it possible to study the effects caused by LSI currents in the frequency domain. Hayashi does not.

Finally, the processing of Hayashi is much longer than that of the invention because Hayashi considers a source mesh by focusing on IR drops. Further, Hayashi requires parallel use of a transit level simulation and a gate-level simulation, making it necessary to use more computing resources, in contrast to the invention.

Although Ha suggests that a triangular waveform be used, the reference does not specify *how* the triangular waveform is applied to an event. The accuracy of a prediction of the EMI noise is dependent on the event in question. The invention discloses this relationship. Hayashi does not.

Finally, Hayashi teaches that a preliminary library listing peak currents, current raising edge times, and current falling edge times be generated. In contrast, in the invention, this information can be back-calculated from information about electric power consumption and transitions existing in ready-made ASIC flows. Thus, this invention provides a high affinity to ASIC flow.

Accordingly, Hayashi does not teach the methods of claims 1 and 28, and thus those claims are patentable over the reference.

Claims 2-27 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hayashi in view of Chen *et al.* ("Power supply Noise Analysis Methodology for Deep-submictron VLSI Chip Design"). For the following reasons, the rejections are respectfully traversed.

First, Chen does not overcome the shortcomings of Hayashi listed above. Chen is directed toward predicting worst-case peak currents, and does not consider EMI noise. Thus, Chen treats current waveform to time-axis modeling roughly, modeling the current peak different from the actual waveform.

Furthermore, Hayashi forms the waveform after the changing-time, whereas the invention forms the waveform to be peak current *during* the changing-time. Hayashi also requires multiplication, in advance, of a predetermined coefficient by the peak current calculated by the transistor level simulation. In contrast, the invention suggests back-calculating using information about electric power consumption and transitions existing in ready-made ASIC flows.

Accordingly, the combination does not result in the invention, as claimed. The combination would use transistor level analysis, resulting in a long processing time. The analysis would be carried out *after* layout, not before, and the EMI accuracy cannot be achieved. Thus, the cited claims are patentable over the combination of references.

Further, the Examiner has not supported a prima facie case of obviousness. Chen does not suggest an "electromagnetic interference analysis method for analyzing the amount of electromagnetic interference arising in an LSI" as in the current application. Instead, by its title and content, Chen is concerned with noise generated by an LSI *power supply*, not noise generated by across an LSI surface, as in the invention. Accordingly, the reference is not reasonably pertinent to the problem with which the inventor is concerned because a person having ordinary skill in the art of LSI EMI emissions would not reasonably have expected to solve that problem by considering a reference dealing with power supply EMI. See *In re Clay*, 966 F.2d 656, 23 USPQ2d 1058 (Fed. Cir. 1992). Thus, Chen is not analogous art.

In addition, the Examiner has not provided the proper motivation for adding the averaging function to Hayahsi. It is not proper to merely find a reference teaching a missing limitation and stating that adding that limitation would be "obvious" because it might provide some benefit. The Examiner must show that there is some suggestion or motivation to modify the reference (MPEP §2143.01). The prior art must suggest the desirability of the combination (Id.). The fact that the claimed invention is within the capabilities of one of ordinary skill in the art is not sufficient, by itself, to establish prima facie obviousness (Id.), and merely listing an advantage of the combination is also not sufficient, as some rationale for combining the references must be found in the references themselves, or drawn from a convincing line of reasoning based on established scientific principles practiced by one skilled in the art that some advantage or beneficial result would be produced by the combination (MPEP §2144). Such motivation cannot be found in the application itself, as such hindsight is impermissible; the facts must be gleaned from the prior art. (MPEP §2142, last paragraph).

Finally, merely adding the averaging function to Hayahsi would not result in a working invention, because there is no suggestion to model and FFT process the result. Hence, the motivation is improper for resulting in a non-working invention.

Hence, there is no proper motivation for combining the references, and thus the rejection is improper.

In consideration of the foregoing analysis, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in a condition for allowance, the examiner is invited

to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 16-0820, our Order No. 32796.

Respectfully submitted,

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